EMSA5-FS

32-bit Embedded RISC-V Functional Safety Processor

The EMSA5-FS is a processor core designed for functional safety. The fault-tolerant processor uses dual or triple instances of the EMSA5, an efficient 32-bit embedded processor IP core implementing the RISC-V Instruction Set Architecture (ISA).

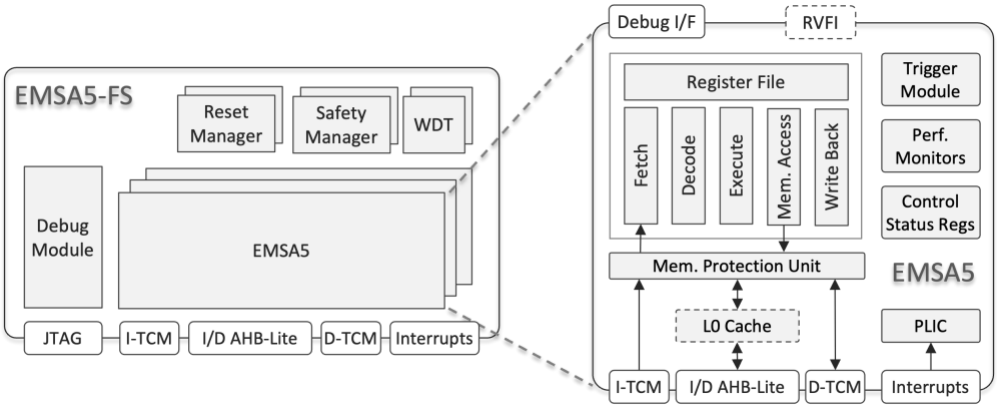
The Harvard architecture EMSA5 processor implements a single-issue, in-order, 5-stage execution pipeline, supporting the RISC-V 32-bit base integer instruction set (RV32I), or the 32-bit base embedded instructions set (RV32E). EMSA5 can support machine and user privilege modes, and optionally the standard Multiply (M), Compressed (C), Control and Status Register (Zicsr), and Instruction-Fence (Zifencei) RISC-V extensions. The processor core uses two tightly-coupled memory (TCM) interfaces (one for data and one for instructions) and communicates with the system via a 32-bit AMBA® AHB-lite bus and its interrupt lines. An optional four-ways set associative cache of configurable size can be attached to the AHB-lite bus.

Designed to meet the most stringent functional safety requirements, EMSA5-FS implements a memory protection unit, employs modular redundancy, uses error correction codes (ECC), and is delivered with sample reset and safety manager modules. Privileged operation modes provide a mechanism to isolate application user-mode processes from each other and from trusted code running in machine mode. The highly configurable memory protection unit enables memory partitioning, which provides protection by restricting access—or limiting the types of access—to memory and memory-mapped modules (e.g., peripherals). ECC protects the memories and buses, and modular redundancy protects the internal processor modules. Finally, the safety manager provides logical and timing supervision and can be customized to meet the requirements of the end application.

EMSA5-FS comes in three versions: EMSA5-FS-T uses triple modular redundancy (TMR), EMSA5-FS-D uses dual modular redundancy (DMR), and EMSA5-FS-L uses DMR in a lockstep setup.

Part of CAST's family of processor cores, the EMSA5-FS processor core has been designed for easy reuse, has been rigorously verified, and is delivered with an ISO 26262 ASIL-D Ready certificate.

Block Diagram



Applications

The EMSA5-FS core is suitable for implementing microcontrollers for devices and systems in automotive, airborne, space, medical and other safety-critical applications.

FEATURES

Designed for Functional Safety

- ISO 26262 ASIL-D Ready Design
- Complete certification package includes FMEDA and SAM documents
- Fail-safe features: Modular redundancy, ECC, reset and safety manager modules
- Memory protection unit with up to 16 regions of configurable size
- Versions: EMSA5-FS-T (TMR), EMSA5-FS-D (DMR), and EMSA5-FS-L (DMR in lockstep)

Embedded RISC-V Processor

- Single-issue, in-order, 5-stage pipeline
- Harvard architecture with separate Instruction and data TCMs and an optionally cached 32-bit AHB-Lite interface
- RV32[I/E][M][C][Zicsr][Zifencei] ISA
  - 32 or 16 32-bit integer registers (16 with the optional E extension)
  - Optional Compressed (16 bit encoding) instructions (C extension)
  - Optional Multiply/Divide instructions (M extension)
- User and Machine Privilege Modes
- Sixteen interrupt lines, extendable with an external interrupt controller, and one Non-Maskable Interrupt (NMI) line

Powerful Debug Features

- Configurable Hardware Performance Monitor
- Support for RISC-V External Debug Support Version 0.13.2 including a Configurable Trigger Module
- Industry-standard JTAG Interface

Easy Software Development and SoC Integration

- Open-source Eclipse-based or commercially available IDEs
- Exploits the wide ecosystem of RISC-V toolchains and libraries
- Available FPGA development kit for rapid prototyping and evaluation
- Optional off-the-shelf platforms integrate the EMSA5-FS core with bus fabric and typical microcontroller peripherals
- On-request custom-tailored integrated platforms using the EMSA5-FS core and interconnect and peripheral cores

Performance and Size

The silicon resource requirements for the EMSA5-FS depend on its configuration. Core configurations using TMR start from 60k gates, and DMR configurations start from 40k gates. EMSA5-FS can run at frequencies exceeding 1GHz on advanced process nodes. Please contact CAST to get implementation data for your target configuration and technology.

Peripherals, Platforms, and Integration Services

IP Integration services are available from CAST to help minimize time to market for systems based on the EMSA5-FS core. The processor core can be delivered pre-integrated with bus infrastructure cores, typical microcontroller peripherals, memory controllers, and interconnect IP from CAST or third parties.

Also, a microcontroller platform comprising of the following components is available off-the-shelf and can be delivered with the EMSA5-FS core:

- Bus Fabric: AHB-Lite with a single master and up to 15 slaves, AHB-Lite to APB bridge, and APB Fabric with a single master and up to 15 slaves
- AHB Peripherals: SRAM Controller, SDRAM Controller
- APB Peripherals: Timers (x2), WDT, GPIO, UART, MSSP (I2C, SPI Master/Slave), QSPI and PLIC

Please contact CAST to learn more details.

Deliverables

The core is available for ASICs in synthesizable System Verilog source code or for FPGAs in optimized netlists. It includes everything required for successful implementation: extensive documentation, a testbench, a sample SoC design, sample synthesis and simulation scripts.

Furthermore, a Safety Manual (SAM), a Failure Modes, Effects and Diagnostics Analysis (FMEDA) document, and the ASIL-D Ready certificate issued by SGS-TÜV Saar GmbH, are delivered with the core.

Support

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.