H264-E-BPS

Low-Power AVC/H.264 Baseline Profile Encoder

altera An Intel Company

The H264-E-BPS IP core is a video encoder supporting the Constrained Baseline Profile of the ISO/IEC 14496-10/ITU-T H.264 standard It Implements an energy-efficient hardware architecture that is optimized for low-latency video streaming at low bit rates.

The H264-E-BPS encoder requires less than half the silicon area of most competing hardware encoders—approximately 125K gates—allowing for very cost-effective ASIC or FPGA implementations. Its small silicon footprint, low external memory bandwidth requirements, and zero software overhead enable H.264 coding at an extremely low energy cost. The encoder is able to process UHD/4K video when mapped on modern ASIC technologies, and Full-HD when mapped on FPGAs.

Despite being small, the H264-E-BPS produces high quality video, especially at low bit rates, and is suitable for systems with low-latency requirements. It uses constant quantization to output video streams of Variable Bit Rate (VBR), or automatically regulates quantization multiple times within a frame to output Constant Bit Rate (CBR) streams. In CBR mode it responds rapidly to temporal or spatial changes in the video content. This can be combined with an artifacts-free Intra-Refresh coding implementation to effectively eliminate bit rate peaks, while preserving the periodic intra-coded references. As a result, the stream buffers can be smaller than those typically required, and the end-to-end latency can be brought down to frame or sub-frame levels. Video quality at low bit rates is preserved, as the encoder intelligently uses block-skipping and quantization coefficient thresholding to reduce bit rate at minimal quality loss, and uses the in-loop deblocking filter to eliminate the blocking artifact.

The core was designed for ease of use and integration. Once initially programmed, it operates without any assistance from the host processor. The encoder's memory interface is extremely flexible: it operates on a separate clock

domain, is independent from the external memory type and memory controller, and is tolerant to large latencies. The core is optionally delivered with a raster-to-block converter, and wrappers for AMBA® AHB, AXI, or AXI-Streaming buses are available.

Customers can further decrease their time to market by using CAST's integration services to receive complete video encoding subsystems. These integrate the encoder core with video and networking interface controllers, networking stacks, or other CAST or third-party IP cores.

The H264-E-BPS IP core is designed using with industry best practices and has been multiple times production proven. Its deliverables include a complete verification environment and a bit-accurate software model.
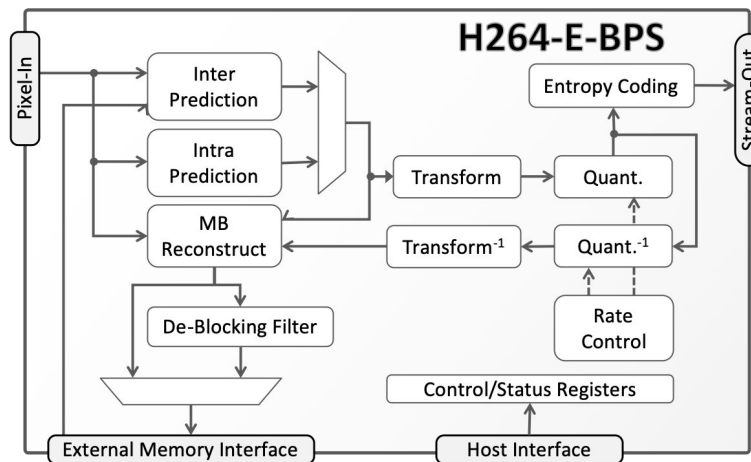
FEATURES

Low-power AVC/H.264 encoder, with small silicon footprint and optimized for low-latency, low-bit-rate video streaming; multiple times production proven

Standard Support
- ISO/IEC 14496-10/ITU-T H.264 Constrained Baseline Profile specification
- Interlaced Video using Main Profile syntax
- Output Annex B NAL byte stream decodable by Baseline, Main and High Profile decoders

Input Video Formats
- Progressive or Interlaced, 4:2:0 YCbCr input with 8 bits per color sample
- Up to Full-HD on Altera FPGAs
- Optional multichannel encoding

Small and Low Power
- 8.6k ALMs & 133k bits of RAM
- Uses less power than competitive hardware H.264 encoders thanks to having under half their silicon footprint and small external memory bandwidth.
- Consumes much less power than any equivalent software, or software-hardware encoder

Low Latency and Low Bit Rates with Fewer Artifacts
- Constant Bit Rate (CBR) output for smaller stream buffers and end-to-end latency
- Advanced rate control regulates Qp multiple times within a frame, and rapidly responds to temporal or spatial video variations
- Enables artifacts-free Intra-Refresh to eliminate bit rate peak of I frames
- Block skipping, Quantized coefficients thresholding, and in-loop deblocking filter improve quality at low bit rates

Ease of Integration
- Zero CPU overhead, stand-alone operation
- Flexible external memory interface uses separate clock, is independent of memory type and tolerant to latencies
- AMBA® Interface Options: DMA-capable AMBA® AHB, AXI or AXI-Streaming

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Coding Tools

- Variable Bit Rate with Constant Qp (VBR-CQP) and Constant Bit Rate (CBR) output with CAVLC Encoding
- Efficient Inter- and Intra- Prediction
  - Motion vector up to –16.00/+15.75 pixels down to ¼ pel accuracy
  - All intra16x16 and most intra 4x4 modes
- Options for improved error resilience
  - Multiple slices per frame
  - Intra-only coding
- Options for better quality at low bit rates
  - Block skipping
  - Deblocking filter
  - Separate quantization values for luma and chrome
  - Thresholding of quantized transform coefficient

Smaller Intra-Only Version

The encoder core can be limited to operate in Intra-Only mode (H264-BIS version). Under this configuration, no external memory is required, and the core's size is further reduced.

The compression efficiency of H.264 Intra-only coding is superior to that of JPEG and comparable to JPEG2000. With Intra-only coding each frame is compressed independently simplifying video editing and enhancing error resilience.

Silicon Resources Utilization

The H264-E-BPS can be mapped to any Altera Family (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following table provides sample implementation data for the core configured under its default configuration (H264-E-BPS) and for the intra-only version for the core (H264-E-BIS).

H264-E-BPS	Area	Memory Bits	DSPs/ MULs	Video Formats *
StratixV	8.6K ALMs	114k	9	1080p30/25 720p60/50/30
Arria10	8.6K ALMs	114k	9	
Max10	21k LEs	112k	13	720p25 480p60

* List of video formats is not exhaustive. Indicated video formats may not be supported at devices of all speed grades

H264-E-BIS	Area	Memory Bits	DSPs	Video Formats *
StratixV	5k ALMs	58K	4	1080p30/25 720p60/50/30
Arria10	5K ALMs	58K	4	
Max10	11K Les	58K	8	480p60

* List of video formats is not exhaustive. Indicated video formats may not be supported at devices of all speed grades

Deliverables

The core is available in source code HDL (Verilog or VHDL) or as a targeted netlist, and its deliverables include everything required for successful implementation:

- Sophisticated self-checking Testbench
- Synthesis scripts.
- Simulation script, vectors and expected results.
- Software (Bit-Accurate Model and test vector generator)
- Comprehensive user documentation.

Evaluation

Potential customers can readily evaluate the video encoder's compression efficiency by using:

- Available sample compressed video streams
- The available Bit-Accurate Model with your choice of input videos
- The Video over IP reference design with video captured over an HDMI interface

Please contact CAST to arrange for your evaluation preference.

Related Cores

The H264-E-BPS is one member of the family of H.264 encoder cores that CAST offers that includes the following members:

- H264-E-HIS: Intra-Only High Profile Encoder
- H264-E-BPF: Ultra-Fast Baseline Profile Encoder
- H264-D-BP: Baseline Profile Decoder
- H264-LD-BP: Low-Power Baseline-Profile Decoder

Please visit www.cast-inc.com to learn more.

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