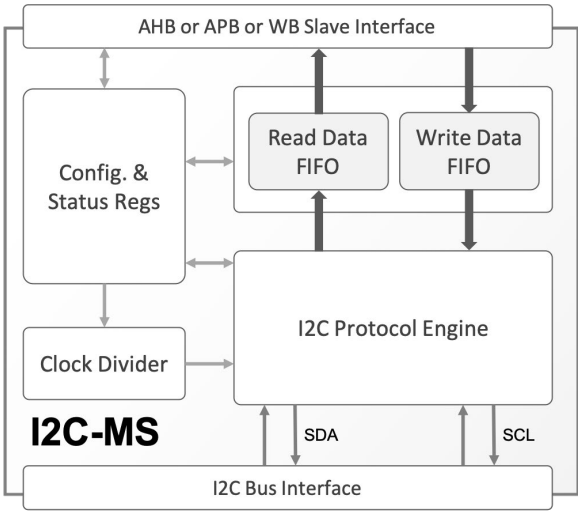
I2C-MS

I2C Master/Slave Controller

The I2C-MS core is a controller for the Inter-Integrated Circuit (I2C) bus. The highly configurable core can implement an I2C bus master, slave, or a combined master and slave, and it communicates with the host via an APB, AHB, or Wishbone slave interface.

The core supports all variations and configurations of I2C networks. It can be used in single- or multiple-master networks, running in any of bus standard-defined speeds, employing a 7-bit I2C slave addressing. Supporting clock stretching, it allows communication between slow slave and fast master.



Designed for ease of use and operation, the core allows choosing between. master and slave operation and setting up I2C transfers at runtime with few register accesses. The core reports its internal status and the I2C bus status via its registers but also with via a rich set of interrupts.

The I2C-MS core is rigorously verified, and silicon-proven. It is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation.

Applications

The I2C-MS core can be used in any application where simple, robust and cost-effective communication is needed. Only one data and one clock line are required to utilize all the benefits of the I2C protocol. Sample scenarios may include communication among host and various sensors, I/O expanders, Data converters, LCD drivers and many more.

Support

The I2C-MS as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

The I2C-MS can be mapped to any Altera FPGA Device (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following sample implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to get characterization data for your target configuration and technology.

Configuration	FPGA Family / Device	Logic (ALMs)	Memory (bits)	Clock Freq. (MHz)
Slave only, 2-bytes FIFOs	Arria® 10 / arria10gx-1	264	32	200
Master only, 2-bytes FIFOs	Arria® 10 / arria10gx-1	316	32	200
Master-Slave, 2-bytes FIFOs	Arria® 10 / arria10gx-1	356	32	200

FEATURES

I2C Bus Protocol Controller

- Compliant to Philips I2C standard
- All I2C bus speeds:
  - Standard-mode (Sm): up to 100 kbit/s, bidirectional
  - Fast-mode (Fm): up to 400 kbit/s, bidirectional
  - Fast-mode Plus (Fm+): up to 1 Mbit/s, bidirectional
  - High-speed mode (Hs-mode): up to 3.4 Mbit/s, bidirectional
  - Ultra Fast-mode (UFm): up to 5 Mbit/s, unidirectional
- 7-bit slave addressing
- Supports single or multi-master buses
- Clock-Stretching to allow fast-master slow-slave communication

Configuration Options

- Operation mode: Master, Slave, or Master/Slave
- Host Interface: APB, AHB, or Wishbone Slave
- Read and Write Data FIFOs depth
- Maximum number of I2C transfers without host intervention

Run-Time Options

- I2C Bus Speed and Clock Frequency
- Master or slave operation (for I2C master/slave core)
- I2C slave addressing mode (for I2C master)

Deliverables

- Synthesizable RTL or FPGA netlist
- Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation