NEWS

CAST

New LZ4 & Snappy IP Core from CAST Enables Fast Lossless Data Decompression

ASIC or FPGA hardware engine offloads a system's CPU for high-throughput, low-latency, lossless data decompression

Woodcliff Lake, New Jersey — **June 4, 2024** — Semiconductor intellectual property provider CAST today announced a new IP core that implements a hardware decompression engine for the LZ4 and Snappy lossless data compression algorithms.

The new LZ4SNP-D LZ4/Snappy Data Decompressor IP core receives compressed data files, detects the LZ4 or Snappy format, performs the appropriate decompression, and outputs the resulting uncompressed data. It has remarkably fast throughput, producing an average of 7.8 bytes of decompressed data per clock cycle in its default configuration.

The core's carefully crafted pipelined datapath enables it to combine this fast throughput with high clock frequency and extremely low latency: the core can run at frequencies exceeding 1 GHz in modern ASIC technologies and over 300MHz in high-end FPGAs and has a processing latency of just 30 clock cycles.

System developers can further increase decompression throughput to rates of 100Gbps or greater by instantiating the core multiple times.

The company believes its LZ4SNP-D is the first available RTL-designed IP core to implement LZ4 and Snappy lossless data decompression in ASICs or FPGAs from all popular providers. "This new decompression core makes it easy and efficient to significantly increase communication bandwidth and data storage capacities while also shrinking memory power consumption," said Tony Sousek, engineering director for CAST. "With it, designers can now build tremendously fast data decompression right into their networking, storage, and other SoCs, enhancing a wide range of applications."

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Systems using the core benefit from its standalone operation, offloading the host CPU from the demanding task of decompressing data. The core handles the parsing of the incoming compressed data files with no special preprocessing. Its extensive error tracking and reporting capabilities ensure smooth system operation, enabling automatic recovery from CRC 32, file size, coding, and non-correctible ECC errors.

The decompression engine core is quite configurable, including IO bus widths, FIFO sizes, maximum history window, and data path width. To further ease integration, the core is natively equipped with AMBA® AXI4-Stream interfaces, which can be bridged to AXI4 or AHB memory-mapped interfaces using DMA engines or interface bridges available from CAST.

The new LZ4SNP-D LZ4/Snappy Data Decompressor IP core is available now. Learn more on its product page, which includes technical details and representative implementation results for ASICs and FPGAs from multiple vendors.

About CAST

Computer Aided Software Technologies, Inc. (CAST) is a silicon IP provider founded in 1993. The company's ASIC and FPGA IP product line includes microcontrollers and processors; compression engines for data, images, and video; interfaces for automotive, aerospace, and other applications; various common peripheral devices; and comprehensive SoC security modules. Learn more by visiting www.cast-inc.com.

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