NEWS

CAST Adds New SafeSPI Controller to its Functional Safety IP Core Product Line

The first such complete core is ideal for protected sensor/processor communication and joins CAST's industry-leading set of ISO 26262 and other automotive cores

Woodcliff Lake, New Jersey — **November 19, 2024**—Semiconductor intellectual property provider CAST, in collaboration with Silesia Devices, today announced a new IP core that implements the Serial Peripheral Interface for Automotive Safety (SafeSPI), an emerging open standard that adds Functional Safety and interoperability features to the de-facto Serial Peripheral Interface (SPI) industry standard.

Why SafeSPI?

Conventional SPI is a four-wire interface for synchronous communication that has been extremely popular, especially for linking sensors with processors in automotive systems. However, there has been no formal industry standard for SPI, and integrating multiple devices into a complex system gets complicated when different developers employ custom SPI variations. Moreover, conventional SPI does not provide for Functional Safety design practices, which is of paramount importance for automotive systems.

In contrast, SafeSPI is a formal industry standard developed and maintained by the SafeSPI Organization, whose members include automotive system leaders Bosch, Continental, and others.

The SafeSPI is an over-SPI protocol that addresses interoperability by allowing only specific implementation options for the lower-level SPI link and providing a detailed specification for all the parameters of the higher-level protocol, such as frame formats and addressing modes. This uniformity eases integration and testing by making communication consistent across diverse devices. SafeSPI further addresses Functional Safety by incorporating key features such as Cyclic Redundancy Check (CRC) for detecting errors in data transmission command and response frames, strict handshaking mechanisms, and fault detection procedures.

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About the New SafeSPI Controller Core

The **SafeSPI-CTRL** SafeSPI Controller Core is the first fully-featured, ASIC or FPGA, SafeSPI 2.0-compliant core with the features required for ISO 26262 ASIL-D Functional Safety certification.

The versatile core can operate as a master, target, or monitor for SafeSPI, or as a master or slave controller for conventional SPI. In addition to operating as a conventional interface controller, the SafeSPI-CTRL can also operate as a SPI-to-AHB bridge that autonomously—without any firmware assistance—translates transactions on the local AMBA® AHB-Lite bus to SafeSPI bus transactions and vice versa.

The SafeSPI-CTRL core supports all the SafeSPI 2.0-specified frame formats and addressing modes, so it can communicate with any SafeSPI-compliant device. It also has extended configuration options for conventional SPI, allowing it to further communicate with devices implementing a wide range of SPI protocol variants or over-SPI protocols.

The core automatically generates and checks CRCs and implements the fault management processes provisioned by the SafeSPI specification, minimizing overhead on the host processor.

Additional hardware options make the core ready for the most stringent Functional Safety assurance level, ISO 26262 ASIL D. These include spatial redundancy for critical modules, data protection by CRC or parity in buffers and registers, and self-diagnostics with a real-time fault injection facility. An optional certification data package facilitates the ISO 26262 certification process for customers; it includes the required FMEDA (Failure Modes, Effects, and Diagnostic Analysis) and Safety Manual documents.

The new SafeSPI-CTRL core implements these Functional Safety features with resource efficiency unmatched by conventional SPI controllers. It is engineered by Silesia Devices and available now through CAST for ASICs and FPGAs, with licensing options including royalty-free. See sample implementation results and more technical details in the SafeSPI-CTRL IP Core product brief.

About CAST

Computer Aided Software Technologies, Inc. (CAST) is a silicon IP provider founded in 1993. The company features one of the broadest and deepest families of Automotive IP cores—including a RISC-V processor and CAN 2.0/FD/XL, TSN Ethernet, LIN, and SENT bus controllers—most of which are Functional Safety certified.

CAST's complete ASIC and FPGA IP product line also includes microcontrollers and embedded processors; compression engines for data, images, and video; interfaces for aerospace, defense, and other applications; various common peripheral devices; and comprehensive SoC security modules. Learn more by visiting www.cast-inc.com.

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