SCR

Smart Card Reader Controller

Implements an interface and controller for communicating between smart cards and host systems using a variety of standard system interfaces.

The SCR supports the ISO/IEC 7816-3:2006 and EMV 4.3 specifications, which define the electrical signals and transmission protocols for smart cards (also known as integrated circuit cards). It acts as a communication controller, passing data to and from the host system and the smart card. It is fully-featured, and can activate and deactivate cards, perform cold/warm resets, handle ATR response reception, and execute other essential functions.

The SCR consists of the core smart card reader logic with a wrapper for the desired system interface. (AMBA APB interface is available; support for AMBA AXI4-Lite, Avalon-MM or Wishbone is optional.)

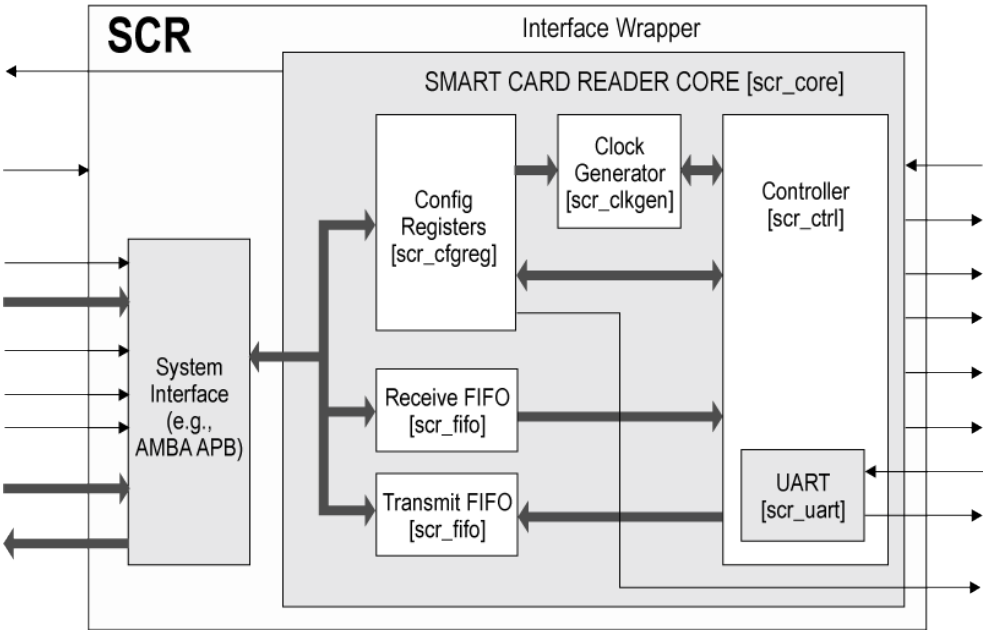
The core is fully synchronous for easier testing and is designed for efficient ASIC or FPGA implementation. This smart card reader core has been rigorously verified and multiple times production proven.

Applications

Smart cards embed a computer chip in a credit-card sized plastic card, and are gaining global popularity for a variety of applications, including:

- personal identification
- mobile phone personalization
- credit/debit functions
- satellite TV security
- health care records storage

Block Diagram



FEATURES

- Supports the ISO/IEC 7816-3:2006 and EMV 4.3 specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Extensive interrupt support system
- Adjustable clock rate and bit (baud) rate
- Configurable automatic byte repetition
- Handles commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission, and
  - T=1 for asynchronous half-duplex block transmission
- Automatic convention detection
- Automatic voltage class selection
- Adjustable FIFOs for Receive and Transmit buffers (up to 32k characters) with threshold
- Configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Standard system interface wrapper architecture for easy integration with host systems
- Fully synchronous design suitable for scan-based testing
- Available as an EDIF netlist optimized for a specific FPGA device or as synthesizable RTL source code

Functional Description

The SCR manages the interactions between an inserted smart card and the host system. It handles all timing issues, and safely transfers data from and to the card.

As shown in the block diagram, the core consists of a main SCR core block which performs according to the 7816 specification, and a wrapper that interfaces the SCR functions to a host system with APB.

SCR Top Level Entity

The wrapper that connects the SCR core to the AMBA APB. It converts the APB signals and makes them useful to the core.

Smart Card Reader Core

Contains five blocks that implement the SCR, and communicates with the host system through the APB wrapper.

Configuration Registers

Store values that provide control over all SCR functions.

Controller with UART

The main functional block, controlling the received and transmitted characters and performing card activation and deactivation, and cold and warm reset.

Includes a UART (Universal Asynchronous Receiver Transmitter) that converts the data from parallel to serial for transmitting from the SCR to a Smart Card and from serial to parallel for transmitting from a Smart Card to the SCR. The UART also performs the guard time, parity checking, and character repeating functions.

Receive FIFO

Stores the data received from the smart card until it is read out by the host system.

Transmit FIFO

Stores the data to be transmitted to the smart card.

Clock Generator

Generates the Smart Card Clock and the Baud Clock Impulse signals, used in timing the SCR.

Implementation Results

SCR reference designs have been evaluated in a variety of technologies. The following are sample results for the APB version, optimized for area and using a two 32x8 FIFOs.

Supported Family	Logic Resources	Memory Resources	Fmax (MHz)	I/Os
Max® 10 10M08SCE144C8G	1,080 LEs	2 RAM Blocks	127	10
Cyclone® 10 LP 10CL006YU256C8G	1,073 LEs	2 RAM Blocks	134	10
Arria® 10 10AS016C4U19I3SG	552 ALMs	2 RAM Blocks	341	10

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation, synthesis, and rigorous code coverage measurements. It has been embedded in numerous shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables

The Altera® FPGA version of this core includes everything required for successful implementation:

- Post-synthesis EDIF netlist or Synthesizable RTL
- Sophisticated, self-checking HDL Testbench including everything necessary to test the core
- Sample driver in C code
- Scripts for simulation
- Comprehensive user documentation, including detailed specifications and design integration guidelines