SPMI-CTRL
MIPI SPMI Controller or Target
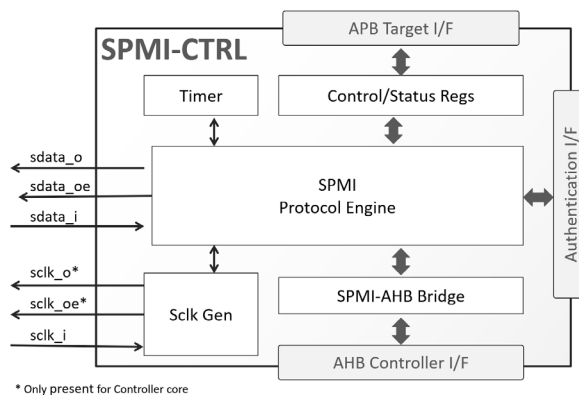
altera
An Intel Company

The SPMI-CTRL core implements a highly featured, easy-to-use controller for the MIPI System Power Management Interface (MIPI-SPMI) bus. It supports the latest version (v2.0) of the MIPI-SPMI specification, and is suitable for the implementation of either Controller or target nodes in an SPMI bus.

The core is designed to minimize the software load on the host processor. Once configured, the core requires no assistance from the host to initialize the bus, connect to bus or disconnect from the bus, grant access of the bus, execute incoming SPMI commands, generate ACK/NACK responses, and check address and data parity.

Although the core only expects the host to provide the outgoing SPMI commands, it provides thorough status information to the host, which can be used for a higher application layer or for debugging purposes. Last received command, outgoing command status, bus status, and node operation status are made available to the host via the core's registers. Parity errors, unknown commands, or failure of receiving node to provide ACK/NACK response are also reported. Furthermore, the core can be programmed to operate in debug mode, under which the core captures and reports all SPMI bus commands regardless of the destination address.

Integration of the core is extremely simple: The core provides access to its registers via a AMBA™ 3 APB target interface, and converts the incoming SPMI read/write commands to accesses on its AHB Controller port. This SPMI-AHB bridging allows easy mapping of the SPMI address space to shared memories or peripheral registers. A dedicated interface

* Only present for Controller core

allows integration with application specific authentication logic, which can be reduced to just hardwiring the authentication response data. The core uses separate clocks for its APB and AHB bus interfaces, and a separate reference clock source for its internal timer. Clocks are independent to each other, with clean clock domain crossing boundaries, and the only requirement is that the AMBA interface clocks have a frequency larger or equal to the maximum SPMI clock frequency.

The core is designed with industry best practices, rigorously verified, and production-proven.

Size and Performance

The SPMI-CTRL can be mapped to any Altera® FPGA device, provided sufficient resources are available. The following table provides sample performance and resource utilization data. Please contact CAST to get characterization data for your target device and configuration.

Configuration	Device Family	Logic Resources	Max, Serial Clock
Arbitration-Capable Controller	Max® 10	1,870 LEs	26 MHz
Arbitration-Capable Controller	Startix® 10, Arria®10	860 ALMs	26 MHz
Request-Capable Target	Max®10	2,160 LEs	26 MHz
Request-Capable Target	Startix® 10, Arria®10	1,065 ALMs	26 MHz

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