TCPIP-1G/10G

1G/10G TCP/IP Hardware Stack

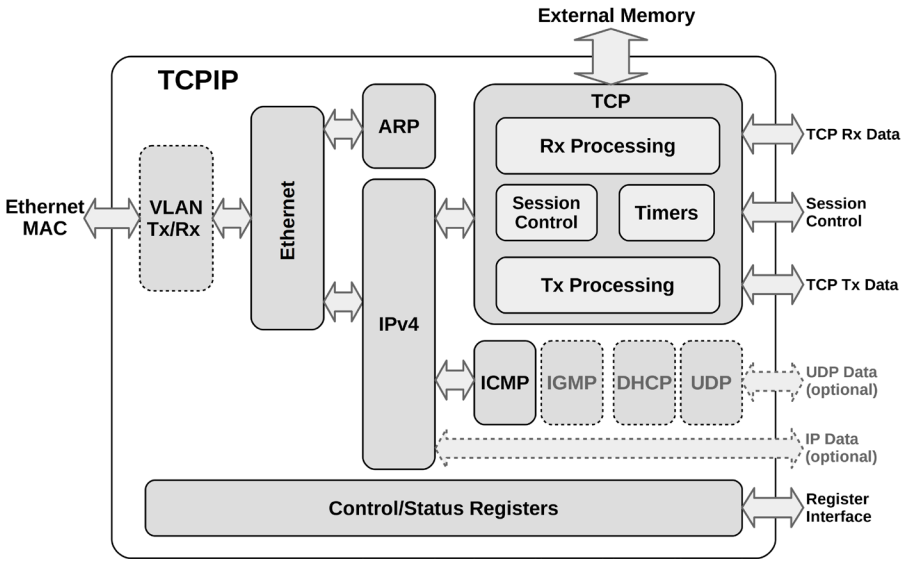
The TCPIP-1G/10G core implements a complete TCP/IP Hardware Protocol Stack. More capable than many offloading engines, it allows systems to connect to an Internet Protocol (IP) network and exchange data using the TCP protocol without requiring assistance from — or even the presence of — a system processor.

The core acts either as a server or a client and, without assistance from the host system, it autonomously opens, maintains, and closes TCP connections. The system integrating the TCPIP-1G/10G core can configure network parameters and preferences by accessing its control registers, and the core is then able to receive and send data via streaming data interfaces.

The highly configurable core can adapt to different applications and diverse system requirements. The maximum number of simultaneous TCP sessions is configurable at synthesis time; it can be as high as 32,768 for devices like data servers, or as small as 1 for edge devices requiring minimum silicon area and power. Further user options include implementing a DHCP client that allows the core to automatically be assigned an IP address, enabling or disabling support of the reassembly of out-of-order TCP packets data, and integrating a UDP hardware stack with multicast support (IGMPv3). Finally, users can choose the packet processing mode, either cut-through or store-and-forward. In cut-through mode, the payload data are delivered to the host system as they arrive without any internal packet buffering and before the packets' integrity can be validated. As a result, the core operating in cut-through mode features extremely low latency and requires less memory, but it cannot reassemble out-of-order packets and it may deliver data that will subsequently be marked as corrupted. Under the store-and-forward mode of operation, the core will always deliver verified, in-order packets, but will have higher latency and require more memory resources.

The TCPIP-1G/10G core is rigorously verified and available in RTL source or as a targeted FPGA netlist. Its deliverables include a testbench, synthesis, and simulation scripts, and comprehensive user documentation.

Block Diagram



FEATURES

Complete TCP/IP Hardware Stack

- 10/100/1000, 2.5G, and 10G Ethernet Transmit and Receive
- TCP server or client with up to 32k simultaneous TCP sessions
- Autonomous and highly efficient TCP connection establishment, maintenance and teardown, retransmission, flow and congestion control
- Optional out-of-order TCP packet reassembly
- Checksums generation and validation
- IPv4 support
- Jumbo and Super Jumbo Frames
- ARP with Cache, ICMP (Ping Reply), VLAN (IEEE 802.1Q),
- UDP, IGMP, and DHCP (optional)

Trouble-Free Operation

- Highly flexible thanks to run-time programmable options including:
  - Local MAC address, IP address, Gateway IP address, and IP subnet mask
  - IP Address, & Port Filters
  - Retransmission timeouts, limits, and enable/disable of fast retransmission
  - Flow control and congestion control
  - Window sizes, MSS
- Non-TCP/UDP IP traffic is optionally forwarded to the system via a dedicated port

Easy SoC Integration

- Standardized AMBA interfaces:
  - 64-bit AXI4-Stream for packet data
  - 32-bit AXI4-Lite for CSR (APB3 optional)
  - 256-bit AXI4 for external memory
- Separate clock domains for packet processing and CSR interfaces
- Independent from external memory type and controller, and from the ethernet MAC or PHY.
- Optionally pre-integrated with AMD FPGA or other third-party eMAC cores

Versions & Configuration Options

- Maximum number of simultaneous TCP sessions (up to 32K)
- Cut-through or store & forward processing

Deliverables

- Synthesizable RTL or FPGA netlist
- UVM Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

Applications

Its high bandwidth, low latency, and autonomous operation make the TCPIP-1G/10G core suitable for a variety of systems, including data and web servers, NIC cards, network security, network storage, electronic trading, industrial systems, and automotive ethernet.

Implementation Results

The TCPIP-1G/10G can be mapped in any AMD device, provide sufficient resources are available. The FPGA resources required for the implementation of the core depend on its configuration. The following table provides sample implementation data for a few out of the many possible configurations of the core.

Configuration						FPGA Resources	
Store & Forward	Max. Sessions	Max. Server Sessions	Max Ports	Max Rules	DHCP Client	Logic (LUTs)	Memory (RAMB)
No	4	2	4	4	Off	19,082	32
No	4	2	4	4	On	20,589	32
Yes	4	2	4	4	Off	22,422	38
Yes	64	32	64	32	Off	23,586	41
Yes	256	128	128	64	Off	26,003	49
Yes	1024	512	256	128	Off	34,315	109

Table 1: FPGA resources requirements for the TCPIP-1G/10G core with one UDP channel per direction, no OoO packet reordering, and clocked at 156 MHz on an ARTIX™ Ultrasclale+ device

The above table does not list all configuration options. Please contact CAST to get characterization data for your configuration and target device.

Functional Description

The TCPIP core receives and transmits TCP packet data and forwards other traffic from the Ethernet MAC to the application and vice versa. It also receives and transmits ARP requests and responses, and responds to ICMP echo reply messages. Optionally the core can also support the UDP and DHCP protocols.

The core consists of the following modules:

- The Ethernet module sends/receives Ethernet frames to/from an external Ethernet MAC, detects the frame type, and multiplexes frames between the protocol stack subsystems.
- The VLAN Tx/Rx module receives Ethernet frames from an external Ethernet MAC, and when enabled detects and compares VLAN tag & filters frames to the correct VLAN tag. In the transmission direction, the module receives Ethernet frames from the Ethernet Frame module and adds the VLAN Tag to the frames when enabled.
- The ARP module sends and receives ARP packets and handles the packets according to command in the packet. It provides the IP-to-MAC address translation services to the IPv4 layers in the protocol stacks.
- The IPv4 module processes the received frames and distributes decoded frames to the related protocol stack modules. Frames from the upper protocol layers are encapsulated into the IPv4 frames and passed to the Ethernet module.
- The TCP module provides the primary functionality of the TCPIP-1G/10G core, i.e. the TCP stack, fully implemented in hardware. The transmit and receive buffers are located in an external memory accessed via the AXI bus.
- The ICMP module supports the echo request response (ping).
- The UDP module is responsible for processing UDP packets for the DHCP module. The module can also provide user UDP channels to the user's design.
- The IGMP module adds the IGMP protocol stack needed for UDP multicast support. The module is optional and requires user UDP channels feature enabled.
- The DHCP module automatically requests and acquires an IP address from a DCHP server. The DHCP feature is optional and requires the UDP module.
- The Control and Status Registers control the core's functionality and report its status.

Support

The TCPIP-1G/10G as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The TCPIP-1G/10G core is available in synthesizable Verilog RTL and FPGA netlist forms. Its deliverable package includes everything required for successful implementation:

- Comprehensive user documentation,
- A highly sophisticated UVM testbench,
- Sample synthesis and simulation scripts, and

Sample designs integrating the TCPIP-1G/10G with third-party or CAST's Ethernet MAC and/or memory controller IP cores are available upon request. Such integrated designs are readily available for devices from all the major FPGA vendors. Please contact CAST to learn more details.