TSN-SE

TSN Ethernet Switched Endpoint Controller

altera An Intel Company

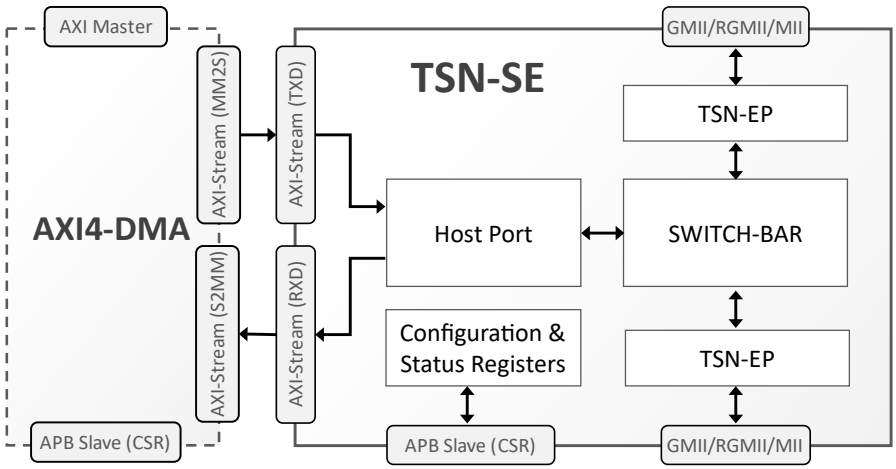
The TSN-SE implements a configurable controller meant to ease the implementation of switched endpoints for Time Sensitive Networking (TSN) Ethernet networks. It integrates hardware stacks for timing synchronization (IEEE 802.1AS-2020), traffic shaping (IEEE 802.1Qav and IEEE 802.1Qbv), frame-preemption (IEEE 802.1Qbu and IEEE 802.3br) and a low-latency Ethernet MAC. Enhanced reliability features can also be supported, using the optional hardware modules for Frame Replication and Elimination for Reliability (IEEE 802.1CB) and Per-Stream Filtering and Policing (IEEE 802.1Qci).

The controller core is designed to enable high-precision timing synchronization and flexible yet accurate traffic scheduling. With cut-through switching and minimal buffering even at the Ethernet MAC level, the TSN-SE features extremely low and deterministic ingress and egress latencies and simplifies the development of time-aware applications. Furthermore, it allows the system to define and tune in real time the traffic shaping parameters according to an application's requirements, and pro-vides the system with timing information (timestamps, alarms, etc.) that is typically required for the operation of a TSN network bridge or endpoint.

The TSN-SE uses standard AMBA® interfaces to ease integration. Its configuration and status registers are accessible via a 32-bit-wide APB bus, and packet data are input and output via AXI-Streaming interfaces with 32-bit data buses. To further expedite and ease the implementation of customer applications, DMA engines providing access to the stream interfaces via a memory-mapped AXI4 master port, and software stacks supporting higher-layer protocols, such as IEEE 802.1Qcc, IEEE 802.1Qca and SNMP, are optionally available.

The TSN-SE is designed with industry best practices and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Block Diagram



Applications

The TSN-SE is suitable for the implementation of TSN Ethernet Endpoints in daisy chained networks (e.g. ring topologies) requiring robust, low-latency, and deterministic communication. Such networks are used in automotive, industrial control, medical, and aerospace applications.

FEATURES

TSN Ethernet Switched Endpoint

- Two Ethernet ports & one host processor port
- Suitable for daisy-chained networks such as rings
- 10/100/1000 Mbps (10Gbps soon)

Low Latency & Flexible Switching

- Low-latency Layer-2 Cut-Through Switching
- Run-time switch configuration enables fast response to network changes
- 802.1Q Tagged VLAN support
- Port-based VLAN
- Configurable VLAN-PCP to TSN-Queue Mapping (QoS by PCP)
- Flexible VLAN and MAC forwarding & filtering
- Configurable MAC lookup table for dynamic and static entries & automatic aging table
- Untagged ports support
- Port Statistics

TSN Features

- Ready for IEEE 802.1AS-2020 (requires light-weight software stack)
- Traffic shaping per IEEE 802.1Qav & IEEE 802.1Qbv with eight TSN-Queues
- Frame preemption per IEEE 802.1Qbu and IEEE 802.3br
- Frame Replication and Elimination per IEEE 802.1CB and Per-Stream Filtering and Policing per IEEE 802.1Qci optionally implemented in hardware
- Path Control and Reservation per IEEE 802.1Qca, and Enhancements to Stream Reservation Protocol per EEE 802.1Qcc optionally implemented in software

Easy System Integration

- AMBA™/AXI4 SoC Interfaces
  - 32-bit APB for register access
  - 32-bit AXI4-Stream for packet data
  - Optional AXI4 DMA engine
- MII, GMII or RGMII, and MDIO Ethernet PHY interface per port
- Requires minimal host assistance for the PTP stack, or no assistance from the host processor when licensed pre-integrated with an embedded processor
- Complete FPGA reference designs available

Implementation Results

The TSN-SE can be mapped to any Altera® FPGA device (provided sufficient silicon resources are available). The FPGA resources requirements depend on the core configuration. The following are sample results for a typical core configuration. Please contact CAST to get characterization data for your target configuration and technology.

Family/Device	Config.*	ALMs	Memory Mbits
Cyclone V 5CSEBA6U19C6	64 Lookup Entries 4kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth No Frame Preemption	11,823	0.42
Cyclone V 5CSEBA6U19C6	126 Lookup Entries 4kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth Frame Preemption	18,434	0.82
Cyclone V 5CSEBA6U19C6	512 Lookup Entries 4kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth Frame Preemption	24,358	1.50

*Partial list of configuration parameters

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The TSN-SE has been rigorously verified, hardware-validated, and proven in real-life environments.

It has also been tested and verified at TSN interoperability plugfests organized by the Labs Network Industry 4.0 (LNI 4.0) association and the Industrial Internet Consortium (IIC).

Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation
- Lightweight PTP stack
- Device driver for FreeRTOS and Linux

Reference FPGA designs with a freeRTOS example software stack with Command Line Interface can be made available on request.

Related Products

The core is a member of CAST's family of automotive interface design IP core products that includes:

- TSN-EP TSN Ethernet Endpoint IP Core
- TSN-SW: TSN Ethernet Switch IP Core
- LLEMAC-1G Low-Latency 10/100/1000 Ethernet MAC IP core
- CAN 2.0/CAN FD/CAN XL Controller IP core
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT / SAE J2716 Transmitter/Receiver Controller IP core

The TSN-SE can be easily integrated with the following IP cores also available from CAST:

- AXI4 DMA engine
- AXI4 Scatter-Gather DMA engine
- UDP/IP 1G/10G Hardware Protocol Stack
- TCP/UDP/IP 1G/10G Hardware Protocol Stack