UDPIP-1G

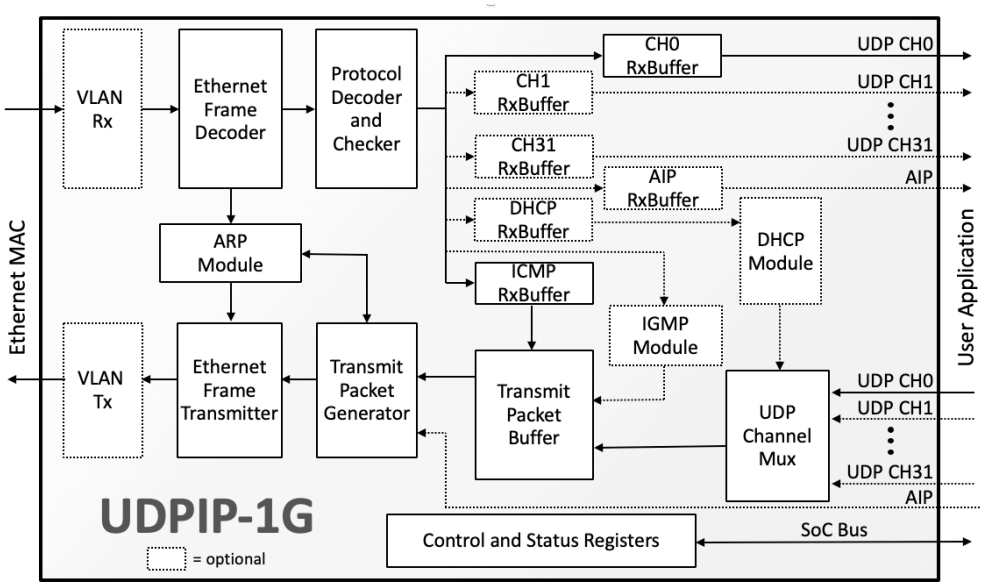
1G UDP/IP Hardware Protocol Stack Core

Implements a UDP/IP hardware protocol stack that enables high-speed communication over a LAN or a point-to-point connection. Designed for standalone operation, the core is ideal for offloading the host processor from the demanding task of UDP/IP encapsulation and enables media streaming even in processor-less SoC designs.

Trouble-free network operation is ensured through run-time programmability of all the required network-parameters (local, destination and gateway IP addresses; UDP ports; and MAC address). The core implements the Address Resolution Protocol (ARP), which is critical for multiple access networks, and the Echo Request and Reply Messages ("ping") of the Internet Control Message Protocol (ICMP) widely used to test network connectivity. It can use a static IP address or automatically request and acquire an IP address from a Dynamic Host Configuration Server (DHCP) server. Furthermore, the core supports 801.1Q tagging, and is suitable for operation in a Virtual LAN.

The core is easy to integrate into systems with or without a host processor. Packet data can be read/written to the core via dedicated AMBA® AXI4-stream or Avalon®-ST interfaces, while registers are accessible via an AXI4-Lite, or AHB or Avalon-MM slave interface. Bridges to other interface protocols can be made available up on request. The core is Ethernet MAC-independent, but can be made available pre-integrated with an Altera, or other third-party eMAC core.

Block Diagram



FEATURES

Complete UDP/IP Hardware Stack

- 10/100/1000 Ethernet on any Altera FPGA device
- IPv4 support without packet fragmentation
- Jumbo and Super Jumbo Frames
- Transmit and Receive
- ARP with Cache
- ICMP (Ping Reply)
- IGMP v3 (Multicast)
- UDP/IP Unicast and Multicast
- UDP Port Filtering
- UDP/IP Checksums generation and validation, and optional Ethernet CRC validation
- VLAN (IEEE 802.1Q) support
- 1 to 32 UDP transmit. and 1 to 32 UDP receive channels
- Ethernet Framing processing for non-UDP user-provided packets
- Optional DHCP client

Trouble-Free Operation

- Run time programmable network parameters
  - Local MAC address, Local IP address, Gateway IP address, and IP subnet mask
  - Per-channel: Destination IP address, Source and Destination and filtered UDP ports, multicast enable/disable and receive group
- ARP support for operation in networks with Dynamic IP allocation

Easy SoC Integration

- Flexible interfaces:
  - Packet Data: 32-bit streaming-capable Avalon-ST or AXI4-Stream
  - Control/Status Registers: Generic 32-bit SRAM-like, or optionally 32-bit AHB, AXI, Avalon-MM or Wishbone
- Separate clock domains for packet processing and control/data interfaces
- Configurable buffer sizes
- Rich interrupt support for system events
- Optionally available pre-integrated with:
  - Altera, or other third-party 1G and 10G eMAC cores
  - CAST Image and Video compression cores

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Functional Description

The UDPIP-1G core receives, and transmits UDP packet data, and forwards other traffic from the Ethernet MAC to the application and vice versa. It also receives and transmits ARP requests and responses, and responds to ICMP echo reply messages. The core generates and validates the UDP and IP checksums of outgoing and incoming packets, respectively. The core can be programmed to discard or forward corrupted packets to the user application.

The core consists of the following modules:

The **Ethernet Frame Decoder** receives Ethernet frames from an external Ethernet MAC, detects the frame type and sends frames to the ARP or the IP packet decoder.

The **Ethernet Frame Transmitter** provides the external Ethernet MAC interface. The transmitter also multiplexes ARP and IP transmit packets from the core subsystems.

The **VLAN Receiver** – receives Ethernet frames from an external Ethernet MAC, detects and compares VLAN tag and filters frames with correct VLAN tag when enabled.

The **VLAN Transmitter** – receives Ethernet frames from the Ethernet Frame Transmitter and adds VLAN Tag to the frames when enabled.

The **Packet Receiver Module** receives IP packets and handles them according to the packet type. The **Packet Decoder** receives IP packets and the decoded packets are stored in the Rx Packet Buffer and then passed to the user application. The **Received Packet Buffer** implements separate data storage for the UDP application data and other data, and its size is configurable at synthesis time.

The **Packet Transmit Module** assembles UDP and ICMP packets. The UDP application data, as well as the ICMP packet data, are stored in the transmit buffer, the size of which is configurable at synthesis time.

The **ARP Module** sends and receives ARP packets and handles the packets according to command in the packet. The **DHCP Module** automatically requests and acquires an IP address from a DCHP server.

The **UDP Channel Demultiplexer** receives UDP packets and demultiplexes them according to a decoded UDP channel number.

The **UDP Channel Multiplexer** receives UDP packet channels from a user application and multiplexes them to the Packet Transmitter module.

Finally, the **Control and Status Registers** controls the core functionality and reports the core status

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

The UDPIP-1G can be mapped to any Altera FPGA device (provided sufficient silicon resources are available). The following sample implementation figures are indicative of the core capabilities and their corresponding utilization metrics. The sample results do not represent the higher speed or smaller area for the core.

Family	UDP Channels	ALMs	Fmax (MHz)	Memory Bits
Arria 10	1	2,857	187	100,352
10AX115S2F45E1SG	4	4,112	190	174,080
Stratix 10	1	3,198	293	100,352
1SG085HN3F43E3VG	4	4,543	277	174,080

Table 1: Sample results for the UDPIP-1G configured with ARP, ICMP, IGMP, 8kB Rx buffer, 4kB Tx buffer, and without DHCP and VLAN

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation.