ZipAccel-D

GUNZIP/ZLIB/Inflate Data Decompressor

ZipAccel-D is a custom hardware implementation of a lossless data decompression engine that complies with the Inflate/Deflate, GZIP/GUNZIP, and ZLIB compression standards.

The core features fast processing, with low latency and high throughput. On average the core outputs three bytes of decompressed data per clock cycle, providing over 1.8Gbps in CerustPro-NX devices. Designers can scale the throughput further by instantiating the core multiple times to achieve higher throughput rates. The latency is in the order of a few tens of clock cycles for blocks coded with static Huffman tables, and typically less than 2,000 cycles for blocks encoded with dynamic Huffman tables.

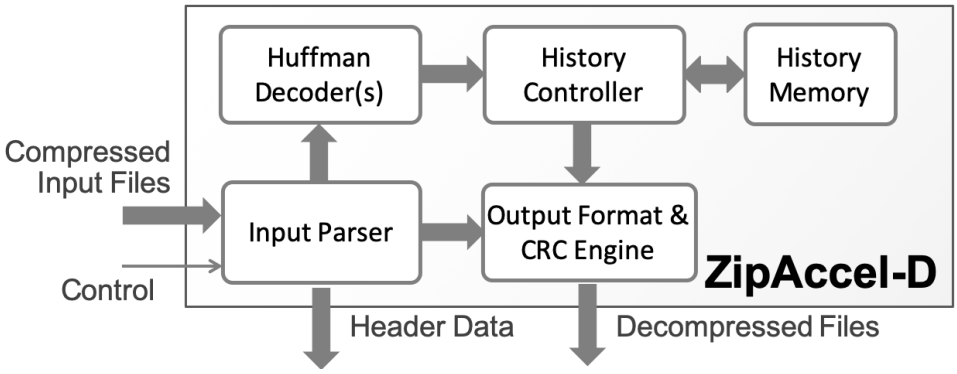
The decompression core has been designed for ease of use and integration. It operates on a standalone basis, off-loading the host CPU from the demanding task of data decompression. The core receives compressed input files and outputs decompressed files. No preprocessing of the compressed files is required, as the core parses the file headers, checks the input files for errors, and outputs the decompressed data payload. Featuring extensive error tracking and reporting errors, the core enables smooth system operation and error recovery, even in the presence of errors in the compressed input files. Furthermore, internal memories can optionally support Error Correction Codes (ECC) to simplify the achievement of Enterprise-Class reliability or functional safety requirements.

The ZipAccel-D core is a microcode-free design developed for reuse in ASIC and FPGA implementations. Streaming data, optionally bridged to AMBA AXI4-stream, interfaces ease SoC integration. Technology mapping is straightforward, as the design is scan-ready, LINT-clean, microcode-free, and uses easily replaceable, generic memory models.

Applications

The ZipAccel-D core is ideal for increasing the bandwidth of optical, wired or wireless data communication links, and for increasing the capacity of data storage in a wide range of devices such as networking interface/routing/storage equipment, data servers, or SSD drives. The core can also help reduce the power consumption and bandwidth of centralized memories (e.g. DDR) or interfaces (e.g. Ethernet, Wi-Fi) in a wide range of SoC designs.

Block Diagram



FEATURES

Compression Standards

- ZLIB (RFC-1950)
- Inflate/Deflate (RFC-1951)
- GZIP/GUNZIP (RFC-1952)

Inflate/Deflate Features

- Up to 32KB history window size
- All Deflate-block types
  - Static and dynamic Huffman-coded blocks
  - Stored Deflate blocks

High Performance & Low Latency

- Three bytes per clock average processing rate, and scalable with multiple core instances.
  - More than 2Gbps with a single core on Avant-E
- Latency from 20 clock cycles for Static Huffman blocks, and typically less than 2000 cycles for Dynamic Huffman blocks

Easy to Use and Integrate

- Processor-free, standalone operation
- Extensive error catching & reporting for smooth operation and recovery in the presence of errors
  - Header syntax errors
  - CRC/Adler 32 errors
  - File size errors
  - Coding errors
  - Huffman tables errors
  - Non-correctable ECC memory errors
- Optional ECC memories
- AXI-stream or native FIFO-like data interfaces
- Microcode-free, LINT-clean, scan-ready design

Configuration Options

- Synthesis time configuration options allow fine-tuning the core's size and performance (partial list):
  - Input and output bus width
  - FIFO sizes
  - Maximum history window
  - Static-only or dynamic and static Huffman tables support

Performance and Area

ZipAccel-D silicon resources requirements and throughput depend on its configuration. Also, ZipAccel-D performance can scale by instantiating more Huffman decoders and by using multiple core instances.

The core can be mapped on any Lattice FPGA provided sufficient silicon resources are available. The following are sample implementation results for two different configurations of the core on a CertusPro-NX and an Avant-E device, and do not represent the smallest possible area requirements nor the highest possible clock frequency.

Configuration			Freq. (MHz)	Logic Resources	Memory Resources	Gbps
In/Out Bit-Width	Huffman Tables	History Window				
64	Static	32,768	82	9,153 Slices	24 EBR	1.97
	Dynamic	32,768	77	26,099 Slices	29 EBR	1.85

Table 1: Sample implementation results for CertusPro-NX (LFCPNX-100, performance grade 9)

Configuration			Freq. (MHz)	Logic Resources	Memory Resources	Gbps
In/Out Bit-Width	Huffman Tables	History Window				
64	Static	32,768	125	6,308 Slices	12 EBR	3.00
	Dynamic	32,768	100	15,365 Slices	17 EBR	2.40

Table 2: Sample implementation results for Avant-E (LAV-AT-500E, performance grade 1)

Contact CAST Sales for help defining likely configuration options and estimating implementation results for your specific system.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has also been embedded in several commercially-shipping products, and is proven in both ASIC and FPGA technologies.

The core has been verified for interoperability with a number of software applications that use GZIP, ZLIB, or Deflate compression.

Deliverables

The core is available in synthesizable HDL (System Verilog) or targeted FPGA netlist forms and includes everything required for successful implementation. Its deliverables include:

- Sophisticated Test Environment
- Simulation scripts, test vectors and expected results
- Synthesis script
- Comprehensive user documentation

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Related Cores

- ZipAccel-C: GZIP/ZLIB/Deflate Data Compression Core
- AXI4-SGMDA: AXI4 to/from AXI4-Stream Scatter Gather DMA
- MM2ST: Memory Mapped to Stream Interface Bridge